H.265 HEVC Decoder IP Core
PRODUCT BRIEF

Overview

The Korusys HEVC decoder core is a highly optimized and parameterisable IP Core targeted exclusively at Altera FPGA technology.

It is an ultra low latency solution, compliant with the ITU-T H.265 standard, designed for applications ranging from High End Broadcast / Contribution and Medical applications through to consumer grade applications.

Korusys provide both the IP core and, as an Altera Design Services Partner, experienced Design Services surrounding the core to implement the most efficient solution for each customer application.

The IP can be provided as a standalone netlist solution for integration into a customer's design, or it can be customized and scaled to a particular implementation.

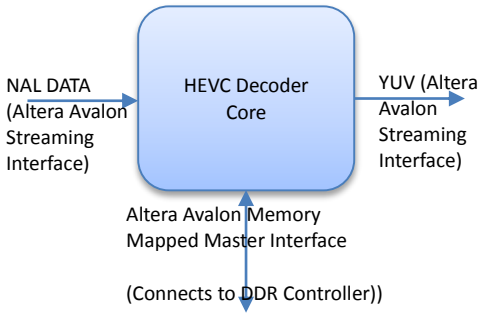

Fig. 1: IP Core Basic Interfaces

The IP core is typically delivered with three simple Altera Avalon Standard Interfaces for simplicity of integration into Customers designs.

Data flow through the IP core is simply NAL data streamed in, DDR is used as a data store and fully decoded YUV data is streamed out.

FPGA Resources

For 4:2:0 8 bit including DDR controller core

- ALM's : ~ 70,000
- Ram : 9 Mbit
- DSP's : 17

Key Features

- Complete stand-alone FPGA solution
- Ultra low latency
- High quality and High precision
- Fully standards compliant, tested with ITU-T conformance streams and bit accurate to HM reference model.
- Provided as IP core or wrapped in custom design as per customer requirements.
- Simple API provided to ease integration.
- Extremely Robust with excellent Error Concealment.

Specifications

- Standard : H.265 HEVC
- Profiles : Main 4.1 / Main 5.0
- Resolutions : Up to 4k
- Frame Rate : 60 fps at HD and UHD
- Chroma : 4:2:2 or 4:2:0
- Precision : 8, 10, 12 or 16 bit
- FPGA : Arria10, StratixV, CycloneV

Ordering Information

To order, or for enquiries, please contact us:

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